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Patents ADP number *(if you know it)*

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If the applicant is a corporate body, give the country/state of its incorporation

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4. Title of the invention REFRESH PIXEL CIRCUIT FOR ACTIVE MATRIX

5. Name of your agent *(if you have one)* WILLIAM E. BIRD of BIRD GOËN and Co

"Address for service" in the United Kingdom to which all correspondence should be sent *(including the postcode)*

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Signature William H. Bird Date 24 June

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# Refresh pixel circuit for active matrix

## Technical field of the invention

The present invention relates to active matrix displays in general, and to active matrix displays with small pixels, such as e.g. LCOS displays, more particularly, as well as to methods of displaying information.

## Background of the invention

A conventional active matrix (AM) is shown in Fig. 1. It comprises a matrix of crossing rows and columns of liquid crystal (LC) pixels $P_1$, $P_2$, ..., $P_n$. At each cross-point of those rows and columns, switching transistors $T_1$, $T_2$, ..., $T_n$ are provided. Every pixel $P_1$, $P_2$, ..., $P_n$ also comprises two capacitors: a storage capacitor $C_{11}$, $C_{21}$, ..., $C_{n1}$ which keeps the voltage across the LC constant between two refresh moments, and an intrinsic (parasitic) pixel capacitance $C_{12}$, $C_{22}$, ..., $C_{n2}$, formed by the liquid crystal stack (pixel electrode - LC - backplate electrode) itself. When the switching transistors $T_i$ of one row are closed (= made conductive), the respective column voltages are stored on the respective storage capacitors $C_{i1}$ of the pixels $P_i$ of that row.

Liquid Crystal on Silicon (LCOS) is a special type of reflective active matrix (AM) liquid crystal displays (LCD), wherein the AM is implemented in a standard silicon process.

A cross-section of a LCOS 1 is shown in Fig. 2. It comprises a semiconductor substrate 2, such as a silicon substrate, with integrated CMOS transistors, and comprises different layers such as a first metal layer 3, a second metal layer 4 and a third metal layer 5 (generally at least four metal layers are provided). On top of the CMOS chip, an LC layer 6 is provided between two alignment layers 7, 8. Thereupon, a glass substrate 9 is provided with an Indium Tin Oxide (ITO) backplate electrode 10, ITO being a conductive and transparent material.

The LC does not operate correctly with a DC voltage, i.e. the pixel voltage has to change in time, the mean value of the pixel voltage (in time) being zero. The electro-optical response of a LC pixel is given in Fig. 3, in a graph in function of the RMS (root-mean-square) voltage. It can be seen that a

certain threshold voltage $V_{th}$ needs to be applied before the LC starts transmitting or reflecting light (depending on the kind of LC).

From the electro-optical response of the LC it can be seen that only a limited part of the curve is suitable for practical implementation. This part is called the "modulation area", and it is located between a threshold voltage $V_{th}$ and an inversion voltage $V_{inv}$. In Vertically Aligned Nematic (VAN) LC types, the threshold voltage $V_{th}$ is typically about 2 V, and the modulation voltage $V_{mod}$ is typically about 1 V. With a constant backplate voltage, the pixel electrode must go over an area of 2*(2 V + 1 V) = 6 V. These voltage values can be quite different for other types of LC.

However, as LCOS is basically a CMOS technology complemented with LC technology, the advantages of CMOS also hold for LCOS. In particular, costs decrease for larger wafers and smaller dimensions of devices on the wafers. At present, in CMOS 0.35 µm processes are used on 8 inch wafers. The maximum gate voltage for transistor devices made in this CMOS process is 3.3 to 3.5 V. This does not seem to be compatible with the voltages required to control the LC.

This problem can be solved by switching the backplate voltage, also called voltage modulation of the common electrode, as described in US-5920298.

In an article of S.C. Tan and X.W. Sun, "P-1: Generic design of Silicon Backplane for LCOS Microdisplays", SID 02 Digest, pp. 200-203, is described the use of voltage modulation of the common electrode in an LCOS display. The voltage on the common electrode is switched between 0 V and the voltage VDD between the two supply rails, in the positive and negative frames respectively. Positive potential across the LC cell is obtained when the voltage applied is referred to the 0 V common cathode, while negative potential is obtained when the voltage on the common electrode is switched to VDD and the applied voltage is less than VDD. This method allows a supply of the same voltage as the LC operating voltage to be used and thus is a low power implementation.

A refresh pixel circuit based on the backplate switching is also described by Tan et al. in the same document. Pixel data from a data line is

transferred via a switch or access transistor towards an intermediate storage capacitor, which holds the image data. An in-pixel buffer serves to replicate the voltage stored on the intermediate storage capacitor on a final storage capacitor, from which the pixel data is put on the pixel electrode. The in-pixel buffer presented in the document is either a PMOS source follower or an NMOS source follower. In both cases there is at least a threshold voltage loss over the in-pixel circuitry transistors, which loss is to be avoided as it decreases the maximum remaining voltage. Moreover, a source follower requires a current source. The current generated by this current source has to be exactly equal all over the chip for each pixel. Another problem is the total power consumption, as pixel count is typically more than 1 million pixels. This can be solved by pulsed current sources, which in turn requires more transistors for each pixel and thus more space on the chip.

**Summary of the invention**

It is an object of the present invention to reduce the area needed by the addressing circuitry underneath a pixel. The area needed is lower than 15 µm x 15 µm, preferably lower than 12 µm x 12 µm, still more preferred it is about 7 µm x 7 µm.

It is a further object of the present invention to provide a display device and a method for transferring image pixel data from an analog memory device to a pixel element of the display device with reduced energy loss.

It is a further object of the present invention to provide a display device and a method for transferring image pixel data from an analog memory device to a pixel element of the display device using less components.

The above objectives are accomplished by a method and device according to the present invention.

The present invention provides an array of pixels, each pixel comprising: a pixel element, a pixel refresh circuit, a first memory element and a first switch element. Each pixel element comprises a first pixel electrode for individual control of the pixel element and a second pixel electrode, the second pixel electrode linking substantially all pixel elements in the array and being connected to a common backplate. The first and second pixel electrode form a

first capacitor. The pixel refresh circuit is intended for transferring electric charge related to a pixel data value from a data input of the pixel to the first pixel electrode via a charge transfer path. The first memory element is coupled to the pixel data input for storing electric charge related to the pixel data value. The first switch element is located between the first memory element and the first pixel electrode, and is for controlling charge transfer from the first memory element through the charge transfer path to the first pixel electrode. According to the present invention, the first switch element and the first memory element co-operate to transfer charge related to the pixel data value passively along the charge transfer path to the first capacitor.

According to an embodiment of the present invention, the array further comprises means for applying a dynamically changing voltage to the common backplate.

According to a further embodiment, charge related to the pixel data value when stored in the first memory element generates a data voltage across the first memory element and the passive charge transfer applies substantially the same voltage as the data voltage on the first pixel electrode.

According to an embodiment, the pixel refresh circuit may further comprise a mirroring circuit, for losslessly mirroring the pixel data value stored on the first memory element to the first pixel electrode of the pixel element. The mirroring circuit may comprise the first switch element having a first and a second data electrode and a control electrode, the first switch element being connected with its first data electrode to an electrode of the first memory element and with its second data electrode to the first pixel electrode, a second memory element for storing data values, the second memory element having a first and a second electrode, the second memory element being connected with its first electrode to the second data electrode of the first switch element, and with its second electrode to the control electrode of the first switch element, and resetting means, for resetting the data value stored in the second memory element.

Alternatively, in an array according to the present invention the pixel refresh circuit of each pixel comprises a plurality of first memory elements, each first memory element being intended to store a pixel data value, each

memory element having a charge transfer path between the plurality of first memory elements and the first pixel electrode, and a plurality of first switch elements, each first switch element for controlling charge transfer from a first memory element through the respective charge transfer path to the first pixel electrode, the first switch elements of one pixel intended to be closed mutually exclusively.

An array according to the present invention may furthermore comprise a second switch element between the first memory element and a data line for providing pixel data values.

The pixel element may comprise a liquid crystal, for example an LCOS element.

The first memory element(s) may be (a) storage capacitor(s).

The second memory element may be a storage capacitor.

The first and second switch element may be a transistor.

The array may be an active matrix.

The present invention also provides a method for refreshing pixel values of an array of pixels, each pixel comprising a pixel element comprising a first pixel electrode for individual control of the pixel element and a second pixel electrode, the second electrode of substantially all pixel elements in the array being connected to a common backplate. The method comprises passively transferring charge related to pixel data to the first pixel electrode.

The step of passively transferring pixel data may comprise losslessly mirroring the data from a first memory element to the first pixel electrode of the pixel element.

According to an embodiment of the present invention, the step of passively transferring pixel data comprises transferring the data from either of a set of memory elements over one switch element from a plurality of mutually exclusively driven switch elements.

These and other features and advantages of the present invention will become apparent from the following detailed description, taken in conjunction with the accompanying drawings, which illustrate, by way of example, the principles of the invention.

**Brief description of the drawings**

Fig. 1 is a schematic diagram of an active matrix according to the prior art.

Fig. 2 is a cross-section of an LCOS device.

Fig. 3 is a graph showing the electro-optical characteristic of a liquid crystal.

Fig. 4 is a schematic representation of a 3-valve optical engine for projecting colour images by means of LCOS pixels.

Fig. 5 is a graph representing the light output of 1 light valve in function of time in case there are 3 light valves, with a small duty cycle (about 33%).

Fig. 6 is a graph representing the light output of 1 light valve in function of time in case there are 3 light valves, with a duty cycle of 100%.

Fig. 7 is a schematic representation of a 1-valve optical engine for projecting colour images by means of LCOS pixels.

Fig. 8 is a graph representing the light output in function of time in case there is only 1 light valve.

Fig. 9 is a graph of the backplate modulation in function of time, and the effect this has on the resulting pixel voltage.

Fig. 10 is a timing diagram of one pixel or row in a backplate switching scheme in a 3-valve optical system.

Fig. 11 is a timing diagram of one pixel or row in a backplate switching scheme in a 1-valve optical system with pulsed light source.

Fig. 12 is a timing diagram of one pixel or row in a backplate switching scheme in a 1-valve optical system with scrolling colour.

Fig. 13 shows a pixel architecture according to a first embodiment of the present invention.

Fig. 14 shows a simulation of the charge transfer in the embodiment of Fig. 12 when the backplate is not being switched.

Fig. 15 shows the relation between the voltage across storage capacitor $C_{S1}$ and storage capacitor $C_{S2}$ of Fig. 12.

Fig. 16 shows a pixel architecture according to a second embodiment of the present invention.

Fig. 17 shows a pixel architecture according a further embodiment of the present invention, which comprises an enhanced data supply to the second embodiment.

Fig. 18 shows a pixel architecture according to yet a further embodiment of the present invention, which comprises an enhanced data supply to the first embodiment.

**Description of illustrative embodiments**

The present invention will be described with respect to particular embodiments and with reference to certain drawings but the invention is not limited thereto but only by the claims. The drawings described are only schematic and are non-limiting. In the drawings, the size of some of the elements may be exaggerated and not drawn on scale for illustrative purposes.

LCOS displays can display colour images. Generally, colour images are made with LCOS pixels in any of two ways: by means of a 3-valve optical engine or by means of a 1-valve optical engine. However, also two-valve optical engines have already been reported, with one LCOS-valve for green, and one LCOS-valve for red + blue.

A schematic representation of a 3-valve optical engine 11 is given in Fig. 4. Incoming light 12 is split by dichroic mirrors 13 into red R, green G and blue B components, and each of these components R, G, B is directed onto LCOS cells 14. The three reflected light beams 15 are brought together again and the compound light beam 16 is projected (in case of projection), or imaged on the retina (in case of near to the eye (NTE) applications). Each pixel is illuminated, either continuously or not, with light of only one colour (Fig. 5 and Fig. 6). In case of projection it is important to have as much light on the projection screen as possible. In this case, the duty cycle will be kept as large as possible, preferably 100% as shown in Fig. 12.

A schematic representation of a 1-valve optical engine is shown in Fig. 7. Alternately the red R, green G and blue B component of the visual spectrum of the light, as shown in Fig. 8 is directed to each pixel of the LCOS matrix (and images). This is called 'temporal multiplexing'. Two systems can be used: pulsed light source or scrolling colour.

In case of 'pulsed light source', the light source is pulsed and sends out alternately the red R, green G and blue B component of the visible spectrum of the light. Possible light sources are LEDs, lasers or conventional light sources provided with an optical system with fast shutters (e.g. LC shutters). All pixels are illuminated with the same colour of light at the same time.

In case of 'scrolling colour', moving colour bands are imaged on the LCOS matrix by means of a suitable optical system. Such optical systems may be a colour wheel 17 for example, as shown in Fig. 7, or a rotating prism (not represented). Each pixel receives subsequently the red R, green G and blue B component of the visible spectrum of the light. However, at each moment, a part of the pixels are illuminated with the red light, while another part of the pixels are illuminated with the green light and still another part of the pixels are illuminated with the blue light. Typically all pixels on one row are illuminated with the same colour of light.

When the backplate (i.e. the ITO electrode 10 on the glass substrate 9) is driven, as represented in Fig. 9, it is possible to use LCs with large threshold voltages $V_{th}$, if the modulation voltage $V_{mod}$ is small enough. By this technique, the AM only needs to provide the modulation voltage $V_{mod}$. It is to be noted that, in order to keep the intensity on a pixel constant over 2 subsequent frames, data and complementary data need to be placed on that pixel (as the backplate switches). The sum of the voltage corresponding herewith ($V_{data}$ + $V_{complementary\_data}$) is a constant depending on the modulation voltage and on the choice of the two backplate voltages between which is switched.

Two configurations can be distinguished: row-at-a-time and frame-at-a-time.

The conventional method of refreshing a display is the row-at-a-time refresh method in which the refresh is carried out on a line-by-line basis while the AM is not illuminated. Once all lines have been written, and thus all pixel electrodes have adopted the right voltage and the LC of each pixel has reached a steady state, the light source becomes active again. A few moments later, the light source is de-activated again, the backplate polarity switches and the display is written again on a line-by-line basis, this time with data corresponding with the new polarity of the backplate. At least the time needed

to write the data in the display can not be used to illuminate the display. This is only useful for 3-valve systems with small duty cycles and with pulsed light sources with small duty cycles. Row-at-a-time does not work with scrolling colour if combined with backplate switching.

In frame-at-a-time, maximum duty cycles are allowed for the light source. This can only be reached if at any moment (thus also immediately after switching of the backplate), the absolute value of the pixel voltage equals the desired RMS voltage. As the backplate is common for all pixels, this requires a frame-at-a-time solution. Frame-at-a-time implies the presence of a memory element in each pixel. The minimum memory element functions are WRITE (analog data is written to the pixel memory element, while the voltage on the pixel electrode remains unchanged) and TRANSFER (the analog data from the memory element is transferred to the pixel electrode; generally, but not necessary, this function destroys the data in the memory cell).

In case of scrolling colour combined with backplate switching, an information update of the pixel electrodes of the whole screen takes place, but also for every line this has to be done when writing a new colour.

For a 3-valve optical system, the information on the pixel electrode is maintained while writing the new data during a WRITE step (Fig. 10). When the bottom line is written, the backplate switches polarity while all pixel electrodes receive (by the TRANSFER step T) their new voltages. The timing diagram of Fig. 10 is thus only valid for all pixels of one row.

For a 1-valve optical system with pulsed light source, the information on the pixel electrode is maintained while new data (a new colour and a new backplate polarity are expected) is written in the memory element during a WRITE step (Fig. 11). When the bottom line has been written, the light source is activated and the backplate changes polarity while all pixel electrodes reach their new voltages (by the TRANSFER) step. Only thereafter, when the LC of every pixel has reached its final value, the light source with a new colour is activated. The timing diagram of Fig. 11 is thus only valid for all pixels of one row. In Fig. 11 the polarity of the backplate changes after every subframe; however, it can also change for example after every frame, or as another example, after every two subframes.

For a 1-valve optical system with scrolling colour, 3 horizontal colour bands move from top to bottom (or inversely) over the display screen. When a certain colour band has just passed a row completely, the pixel electrode voltages of that row are adapted to the voltages for the new colour, which has been written in the meantime. This is done by a WRITE + TRANSFER step. Immediately thereafter, the complementary data is written in the memory cells of these pixels by means of a WRITE step (Fig. 12). The switching of the backplate can take place at any moment, provided that no two TRANSFER steps follow each other, or, with other words, a TRANSFER step needs to be preceded by a WRITE step. This means that the backplate can switch maximum once per subframe (this is what is illustrated in Fig. 12). Less than once per subframe is also possible, e.g. once per frame.

A pixel architecture according to a first embodiment of the present invention is shown in Fig. 13. It comprises three separately driven switch elements in series, namely transistors M1, M2, M3 and uses the backplate switching technique. The main advantage of backplate switching is the reduction in processing cost: the low voltage range enables the use of cheaper IC technologies. This circuit overcomes one of the big disadvantages of backplate switching applied to the basic single pixel single storage architecture, namely, the illumination duty cycle is maximised, thereby improving the overall light throughput of the display system. Also the number of components is low which allows formation of the control circuitry in a small pixel area, i.e. less than 15 x 15 = 225 micron$^2$, more preferably equal to or less than 12 x 12 = 144 micron$^2$, and most preferably, equal to or less than 7 x 7 = 49 micron$^2$. There are two memory elements, namely storage capacitors $C_{S1}$ and $C_{S2}$. Storage capacitor $C_{S1}$ has a first electrode connected between the first switch element M1 and the second switch element M2, and a second electrode connected to a fixed voltage level, such as ground for example. Storage capacitor $C_{S2}$ is floating, which imposes an extra mask or step for the IC processing (CAPA-implant or double poly technology). It has a first electrode connected between the second switch element M2 and the third switch element M3, and a second electrode connected to a driving electrode of the second switch element M2. Storage capacitor $C_{S2}$ holds the image data

during a frame, while the other storage capacitor $C_{S1}$ is being updated with the data of the next frame. After the backplate is switched, the new image data is transferred from $C_{S1}$ to $C_{S2}$ along a charge transfer path. A characteristic of the circuit is that it implements an 'analog shift register': the signal transfer from $C_{S1}$ to $C_{S2}$ occurs without a loss in signal amplitude. The loss-free signal transfer along the charge transfer path requires two more transistors which complicates somewhat the driving of the active matrix (two more signals (fi2 and fi3) per row which are supplied by the timing circuit, not shown).

The sequence of operations performed when displaying data in an LCOS pixel controlled by a pixel architecture as shown in Fig. 13, is as described below. Fig. 14 shows a simulation of the charge transfer (the backplate is not being switched in this example). In the following all drive signals are provided by a timing circuit (not shown).

During a WRITE step, the data voltage is transferred from the column col to the first memory element, namely storage capacitor $C_{S1}$. This requires the activation of the first switch element, namely transistor M1 through gate signal 'row'. This operation corresponds to the storing of the next frame contents.

Then follows a TRANSFER step. First, at $t_1$, comes the activation of another switch element, namely transistor M3, as preparation for the actual lossless transfer. At that moment, the voltage on the gate of the second switch element, transistor M2, is at low potential, e.g. 0 V. The storage capacitor $C_{S2}$ has a voltage dropped across it which is determined by $V_{reset}$. Once storage capacitor $C_{S2}$ has been reset by transistor M3 (at $t_2$, the gate of M3 goes back to ground potential), activation of another switch element at $t_3$, namely transistor M2, discharges $C_{S2}$ by as much as transistor M2 allows before this switch element shuts off. When switching on M2 at $t_3$, fi2 goes high, e.g. to $V_{DD}$, and $V_{mirror}$ immediately follows due to the charge on $C_{S2}$. The mirror voltage peaks up to e.g. 8V for a short while (~20ns); the height of this peak can be reduced by increasing the rise time of V(fi2): in the present example of Fig. 14 it was set to 1ns, other examples with 10ns rise times show peak voltages just above 6.5V. This is because $C_{S2}$ is given time to discharge while M2's gate is still rising.

Part of the charge on $C_{S2}$ flows towards $C_{S1}$ along the charge transfer path, as can be seen from parts 20 and 21 of the graph of Fig. 14. The voltage on $C_{S1}$ cannot exceed fi2-$V_{th}$, assuming all conditions are met for a positive charge transfer towards $C_{S1}$. Switching off transistor M2 at $t_4$, makes the mirror voltage $V_{mirror}$ become equal to the voltage previously stored on storage capacitor $C_{S1}$. At this moment, the TRANSFER step has taken place, as the value which previously had been written on storage capacitor $C_{S1}$ is now put on the pixel electrode.

In a next step, at $t_5$, switch element transistor M1 is activated by applying a high voltage, e.g. $V_{DD}$, to "row". Data voltage is transferred from the column "col" to the first memory element, namely storage capacitor $C_{S1}$, and thus data for the next frame is stored during this WRITE step. At $t_6$ the switch element transistor M1 is deactivated again, and a TRANSFER step as explained above can be carried out.

The circuit operation can be summarised as follows: the memory element, namely storage capacitor $C_{S2}$ is pre-set to a reference voltage $V_{ref,S2}$ and switch element M2 makes storage capacitor $C_{S2}$ charge up the further memory element, namely storage capacitor $C_{S1}$ by an amount limited to exactly $V_{ref,S2}$-$V_{data}$. The resulting voltage across storage capacitor $C_{S2}$ is then $V_{ref,S2}$ [preset] – ($V_{ref,S2}$-$V_{data}$) [amount gone to $C_{S1}$] = $V_{data}$. It is to be noted that $V_{data}$ equals the modulation portion of the LC driving voltage. The threshold portion $V_{thlc}$ is obtained by switching of the backplate.

The relative sizes of the storage capacitors $C_{S1}$ and $C_{S2}$ should be chosen correctly in conjunction with the voltage levels Vrow, fi2, fi3 and Vreset. To illustrate the operating limits, the relation between the voltage across $C_{S1}$ and $C_{S2}$ is shown in Fig. 15. Three operating regions can be noted: one of clamping by the M2 terminal substrate diode on the 'mirror' node, a second linear region where the data voltage is amplified by a factor ($C_{S2}$+$C_{LC}$)/$C_{S1}$ and a third saturation region where M2 can never get into conduction.

Preferably, a terminal diode of transistor M2 at the side of the pixel electrode (mirror) prohibits negative voltages. $V_{mirror}$ can become negative e.g. when $C_{S1}$ is very large compared to $C_{S2}$ and when $C_{S1}$ is at a low potential: turning on M2 will then completely discharge $C_{S2}$ to a low voltage level.

Turning off $C_{S2}$ would 'push' the mirror voltage below zero, if the terminal diode wasn't there. Preferably the values of $C_{S1}$ and of $C_{S2}$ are equal, and $C_{LC}$ is much smaller than $C_{S2}$.

The linear region is characterised by the amplification of $V_{data}$ by $(C_{S2}+C_{LC})/C_{S1}$.

Backplate switching is done before the charge transfer to zero out an error voltage resulting from the finite ratio between $C_{S2}$ and $C_{LC}$. In addition, this eliminates a dependency on the exact ratio of storage capacitance $C_{S2}$ and pixel capacitance $C_{LC}$. However, once the backplate has been switched, it must still be possible for transistor M3 to reset $C_{S2}$: $V_{data,max} + V_{pp,backplate} \times C_{LC}/(C_{LC}+C_{S2}) <= fi3-V_{th}$. In other words, fi3 must be large enough to reset $C_{S2}$ even after switching of the backplate.

A further embodiment of the present invention is shown in Fig. 16. This circuit provides every pixel with a second or 'shadow' memory element, namely a storage capacitor that stores the voltage for a next frame with e.g. opposite electrical polarity, and with a second or shadow charge transfer path. While the 'shadow' memory element is being refreshed, the 'active' memory element drives the complete pixel matrix. Together with the backplate voltage the active memory element connected to the pixel array (AM) creates a pattern of electrical fields of one polarity across the liquid crystal. The two electrodes (backplate and pixel) form a capacitor $C_{LC}$; the capacitance is a function of the LC layer and often this capacitor is non-linear. Switching the backplate to another voltage causes the electrical field to change and switching to an adequate voltage can even cause the electrical field to change polarity. Switching of the backplate voltage is intended to result in an alternating electrical field across the LC. The pattern of electrical fields is changed, and the resulting image is no longer correct. Therefore, the shadow memory element stores the voltages needed to obtain the correct electric fields (opposite electrical polarity) after switching the backplate voltage. The fact that backplate switching can be applied leads to a significant reduction in the required voltage range of the pixel electrode. The presence of the shadow memory element avoids scanning of the complete AM after backplate switching. As a result the switching can be done within a relatively short time

window. The shadow memory element results in maximising the time window during which the pixel voltages are correct, or in other words: results in a maximum illumination duty cycle.

Although two memory elements per pixel and two charge transfer paths per pixel are shown, the present invention is not limited thereto. The switch elements, namely transistors SA, SB, MA, MB can be of either n- or p-type; however, n-types usually have higher mobility parameters, so they are faster and preferred. Floating p-types may be advantageous because the body effect is minimised; however, there is always a loss of one threshold voltage Vt with a single transistor switch circuit and the amplitude of the column voltage is always limited to the maximum gate voltage minus Vt. The memory elements, namely storage capacitors Csta, Cstb can be non-floating, this simplifies the requirements for or the cost of the IC technology (e.g. a double poly technology is not needed).

The readA and readB signals, applied at the gates of two switch elements, namely, transistors MA and MB respectively, are basically each others' inverse. They connect the pixel electrode on turns with storage capacitor Csta and with storage capacitor Cstb. The two series of storage capacitors form a double memory element structure, which will be called $D^2RAM$. DRAM_a is a memory element which stores the voltage levels for one frame (e.g. of one polarity), while DRAM_b is a memory element being updated with the voltage data for the next frame or subframe (e.g. of opposite polarity or of other colour). In practice the two signals readA and readB should not be active simultaneously to eliminate a non-desirable charge transfer between the two DRAMs.

When the readA signal is high or active, the memory element DRAM_a drives the pixel matrix (the data of storage capacitor Csta is put on the corresponding pixel element $C_{LC}$) and updating of the storage capacitor Csta is disabled ('rowA' signal is inactive). While the memory element DRAM_a is driving the corresponding pixel element $C_{LC}$, the contents of the DRAM_b matrix is being updated.

During a WRITE + TRANSFER step, readA is high or active and readB is low or inactive. Also rowB is low or inactive. ReadA is high or active until

Csta has reached the desired voltage. Alternatively, during the WRITE + TRANSFER step, readB is high or active and readB is low or inactive. Also rowB is low or inactive. ReadA is high or active until Csta has reached the desired voltage.

During a WRITE step, if readA was high or active, then rowB is brought to a high or active status, until Cstb has reached the desired voltage, given by the data value on the data line col. If readB was high or active, then rowA is brought to a high or active status, until Csta has reached the desired voltage, given by the data value on the data line col.

During a subsequent TRANSFER step, if readA is in a high or active state, the readA is brought to low or inactive. ReadB is brought to high/active, until a next TRANSFER or WRITE + TRANSFER step. If readB was in a high or active state, the readB is brought to low or inactive, and readA is brought to high/active, until a next TRANSFER or WRITE + TRANSFER step.

Only 4 low voltage switch elements, namely transistors SA, MA, SB, MB and two low voltage memory elements, namely storage capacitors Csta, Cstb are needed for the circuit of Fig. 16. The storage capacitors Csta, Cstb can be implemented as gate capacitors. The capacitance density of these capacitors is higher compared to double poly, medium to high voltage storage capacitors. With two transistors in series, the same bulk effect is present as with the classical DRAM architecture, because the data voltage never exceeds Vmax(gate)-Vt. The pixel switch could be implemented with CMOS switches, but this doubles the number of transistors and requires the presence of biased wells and their clearing area – this solution costs more than double the area.

The idea of two parallel circuits driving/underneath the pixel matrix, can be extended to provide more parallelism. The idea can be of interest for static AMs or purely digital AMs (e.g. for driving Ferro-electric Liquid Crystals (FLCs)).

The combination of different single panel colour schemes and backplate switching can be used with the above mentioned AM embodiments as long as the refresh speed is high enough. The degree of increase in refresh speed depends on the minimum speed required to mitigate colour break-up effects

and on the colour scheme used. The smallest increase is with frame sequential colour schemes.

With the classic DRAM-like AM, the light output with frame sequential colour is reduced by the duty cycle of the panel illumination and reduced by the >60% loss of white light in the colour filter. However, embodiments of the present invention described above as a $D^2RAM$ architecture allow a quasi-simultaneous update of all pixel voltages. This means the duty cycle in a frame sequential colour scheme can be very close to 100%. The frame rate needs to be at least 3x the frame rate in a triple panel set-up. Higher rates can be desirable to reduce colour break-up artefacts.

The scrolling colour (colour wheel) and rotating prism schemes (known from Philips) are improvements over the classic DRAM frame sequential colour scheme, because the light throughput is larger. The colour wheel can be combined with a colour recuperation technique that avoids the 60% loss. The rotating prism does not use a colour filter, but a 'colour separator' so that less or no light power is wasted.

Applying backplate inversion requires both DRAMs' to be updated. This way backplate inversion can be done at any moment. However, this requires double the frame rate: either a double column pixel layout must be foreseen or a column driver with two times as much parallellism.

According to a further embodiment, which is an amendment to the circuit of Fig. 16, data and complementary data are stored simultaneously on memory elements, namely storage capacitors C1 and C2. A diagrammatic representation of a circuit corresponding to this embodiment is given in Fig. 17. This embodiment allows the number of row signals to be decreased to one for every row. An advantage thereof is that for some control schemes, e.g. for scrolling colour with backplate switching, the sequence WRITE + TRANSFER followed by WRITE is replaced by one simultaneous action, more particularly switch elements M1 and M3 are simultaneously open and either the switch element M2 is open and switch element M4 is closed, or the inverse. The TRANSFER action then comprises the following: if M2 was open, then M2 is closed and thereafter M4 is opened; if M4 was open, then M4 is closed and thereafter M2 is opened. The replacement of 2 actions (WRITE + TRANSFER

followed by WRITE) by 1 action has an important impact on the design of the column driver. Because data and complementary data are always put on the memory elements, namely storage capacitors simultaneously, the data stream (bandwidth) in the column driver can be reduced to one half with respect to the conventional method, by using differential analog electronics (opamp) with about the same complexity.

According to yet a further embodiment, the circuit of Fig. 13 can be amended in an analogous way. The result is shown in Fig. 18. Here also, the data and complementary data are put simultaneously on the memory elements, namely storage capacitors C5, C6 respectively. An advantage of this embodiment is that with certain control schemes, e.g. scrolling colour with backplate switching, the sequence WRITE + TRANSFER followed by WRITE, in which the column driver is active twice, is replaced by the sequence WRITE and TRANSFER. The WRITE step then consists of opening two switch elements, namely transistor M9 and transistor M10; while all other switch elements (transistors in the figure) are kept closed. This stores data on the memory elements, namely storage capacitors C5 and C6 respectively. The TRANSFER step then consists of, if the data on storage transistor C5 has to be transferred, opening switch element M11, while switch element M12 is kept closed; and if the data on storage transistor C6 has to be transferred, opening M12 while M11 is kept closed. Thereafter the method as explained above with regard to Fig. 13 is followed. Replacing the sequence of 2 actions by 1 action has the same impact on the design of the column driver as in the previous embodiment.

While the invention has been shown and described with reference to preferred embodiments, it will be understood by those skilled in the art that various changes or modifications in form and detail may be made without departing from the scope and spirit of this invention.

CLAIMS

1.- An array of pixels, each pixel comprising:

a pixel element, each pixel element comprising a first pixel electrode for individual control of the pixel element and a second pixel electrode, the second pixel electrode linking substantially all pixel elements in the array and being connected to a common backplate, the first and second pixel electrode forming a first capacitor,

a pixel refresh circuit, for transferring electric charge related to a pixel data value from a data input of the pixel to the first pixel electrode via a charge transfer path,

a first memory element coupled to the pixel data input for storing electric charge related to the pixel data value,

a first switch element located between the first memory element and the first pixel electrode for controlling charge transfer from the first memory element through the charge transfer path to the first pixel electrode,

wherein the first switch element and the first memory element co-operate to transfer charge related to the pixel data value passively along the charge transfer path to the first capacitor.

2.- An array according to claim 1, further comprising means for applying a dynamically changing voltage to the common backplate.

3.- An array according to claim 1 or 2, wherein charge related to the pixel data value when stored in the first memory element generates a data voltage across the first memory element and the passive charge transfer applies substantially the same voltage as the data voltage on the first pixel electrode.

4. - An array according to any of claims 1 to 3, the pixel refresh circuit further comprising:

a mirroring circuit, for losslessly mirroring the pixel data value stored on

the first memory element to the first pixel electrode of the pixel element.

5.- An array according to claim 4, wherein the mirroring circuit comprises the first switch element having a first and a second data electrode and a control electrode, the first switch element being connected with its first data electrode to an electrode of the first memory element and with its second data electrode to the first pixel electrode,

a second memory element for storing data values, the second memory element having a first and a second electrode, the second memory element being connected with its first electrode to the second data electrode of the first switch element, and with its second electrode to the control electrode of the first switch element, and

resetting means, for resetting the data value stored in the second memory element.

6.- An array according to claim 1, 2 or 3, the pixel refresh circuit of each pixel comprising:

a plurality of first memory elements, each first memory element being intended to store a pixel data value, each memory element having a charge transfer path between the plurality of first memory elements and the first pixel electrode, and

a plurality of first switch elements, each first switch element for controlling charge transfer from a first memory element through the respective charge transfer path to the first pixel electrode, the first switch elements of one pixel intended to be closed mutually exclusively.

7.- An array according to any of the previous claims, furthermore comprising a second switch element between the first memory element and a data line for providing pixel data values.

8.- An array according to any of the previous claims, wherein the pixel element comprises a liquid crystal.

9.- An array according to claim 8, wherein the pixel element comprises an LCOS element.

10.- An array according to any of the previous claims, wherein the first memory element(s) is (are) a storage capacitor(s).

11.- An array according to claim 5 or any claim depending on claim 3, wherein the second memory element is a storage capacitor.

12.- An array according to any of the previous claims, wherein the first switch element is a transistor.

13.- An array according to any of claims 7 to 12, wherein the second switch element is a transistor.

14.- An array according to any of the previous claims, wherein the array is an active matrix.

15.- A method for refreshing pixel values of an array of pixels, each pixel comprising a pixel element comprising a first pixel electrode for individual control of the pixel element and a second pixel electrode, the second electrode of substantially all pixel elements in the array being connected to a common backplate, the method comprising passively transferring charge related to pixel data to the first pixel electrode.

16.- A method according to claim 15, wherein the step of passively transferring pixel data comprises losslessly mirroring the data from a first memory element to the first pixel electrode of the pixel element.

17.- A method according to claim 15, wherein the step of passively transferring pixel data comprises transferring the data from either of a set of memory elements over one switch element from a plurality of mutually

exclusively driven switch elements.

**ABSTRACT**

## Refresh pixel circuit for active matrix

The present invention provides an array of pixels, each pixel comprising: a pixel element, a pixel refresh circuit, a first memory element and a first switch element. Each pixel element comprises a first pixel electrode for individual control of the pixel element and a second pixel electrode, the second pixel electrode linking substantially all pixel elements in the array and being connected to a common backplate. The first and second pixel electrode form a first capacitor. The pixel refresh circuit is intended for transferring electric charge related to a pixel data value from a data input of the pixel to the first pixel electrode via a charge transfer path. The first memory element is coupled to the pixel data input for storing electric charge related to the pixel data value. The first switch element is located between the first memory element and the first pixel electrode, and is for controlling charge transfer from the first memory element through the charge transfer path to the first pixel electrode. According to the present invention, the first switch element and the first memory element co-operate to transfer charge related to the pixel data value passively along the charge transfer path to the first capacitor.

The present invention also provides a method for refreshing pixel values of an array of pixels

+ Fig. 13

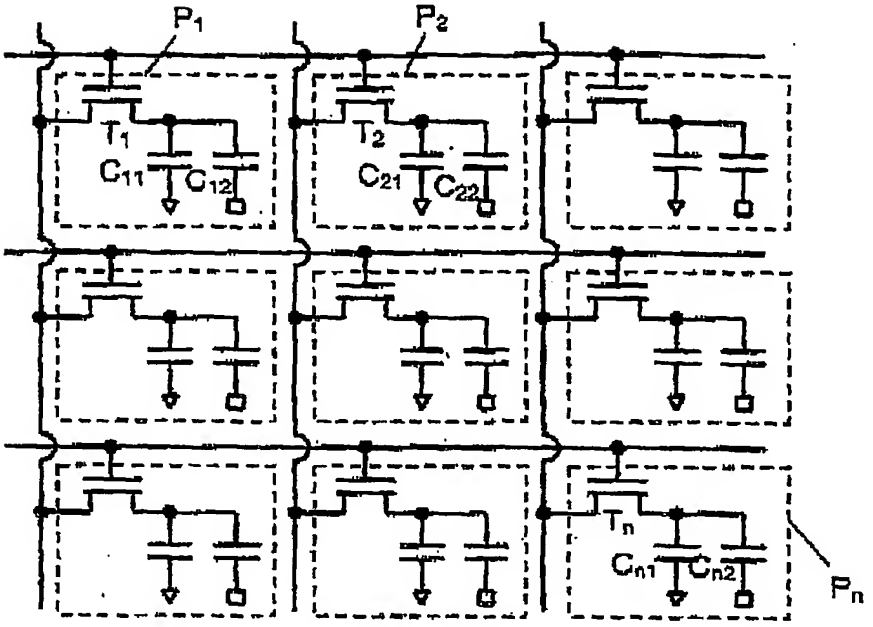


Fig. 1 - Prior Art

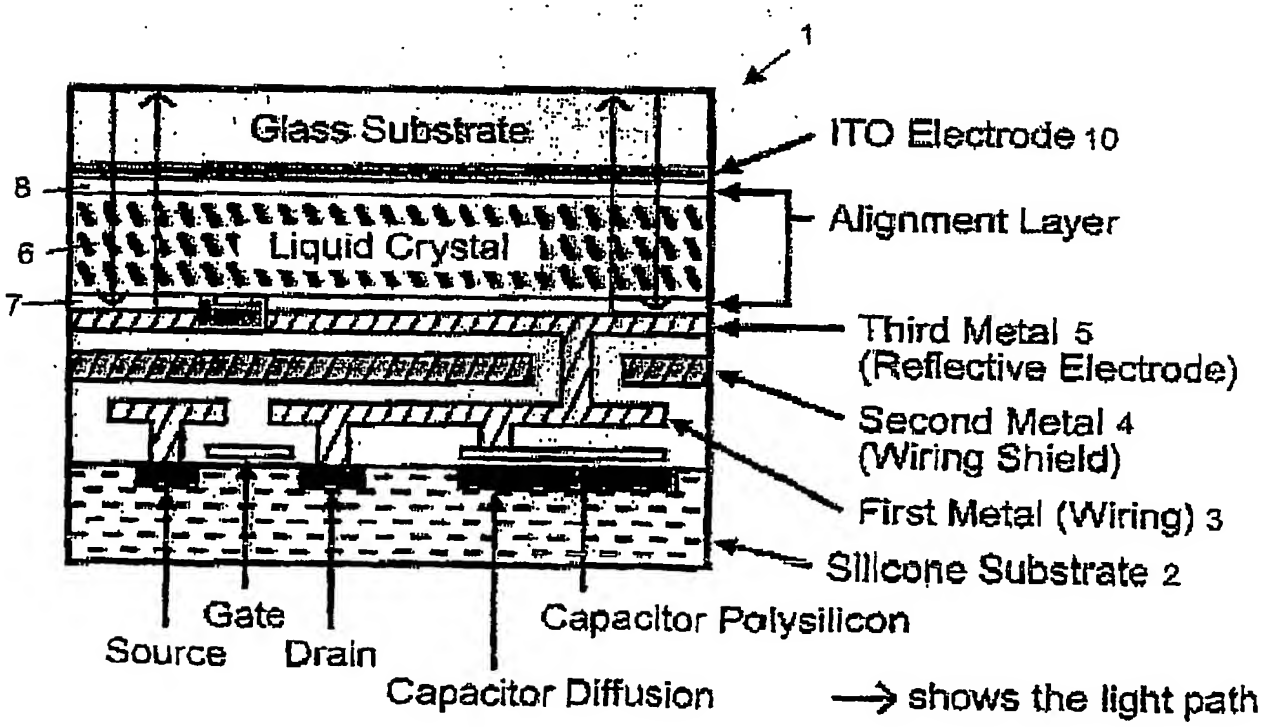


Fig. 2

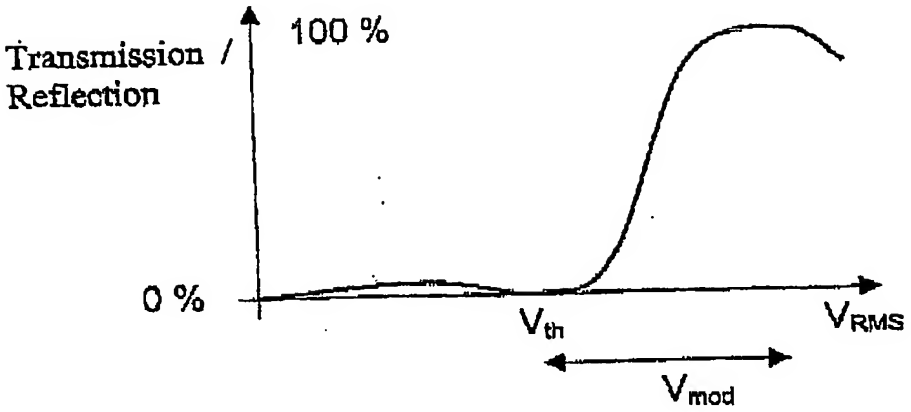


Fig. 3

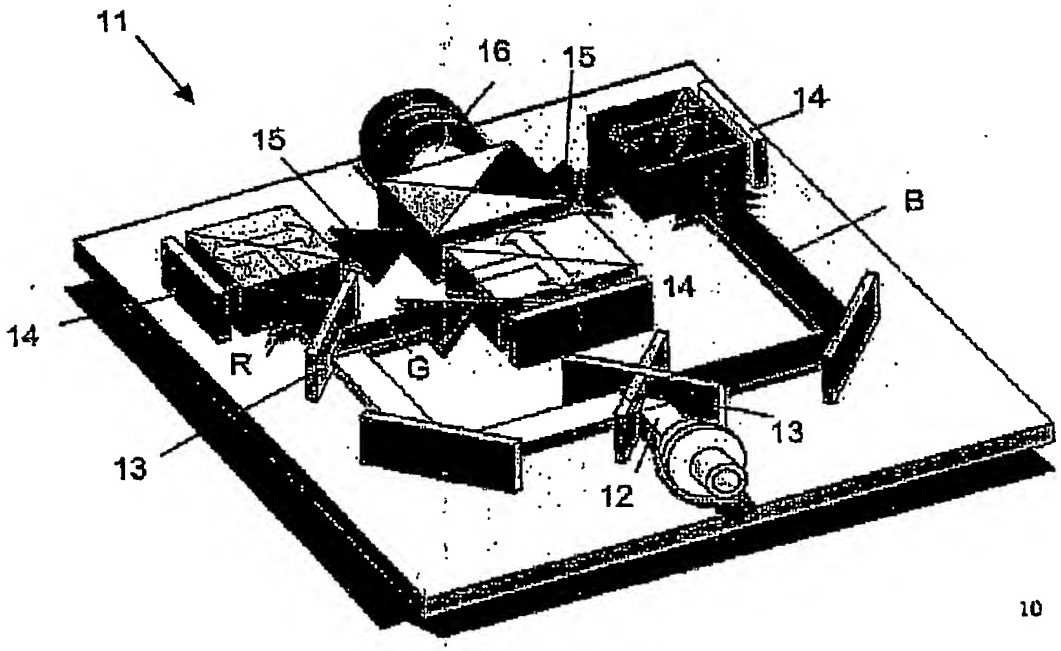


Fig. 4

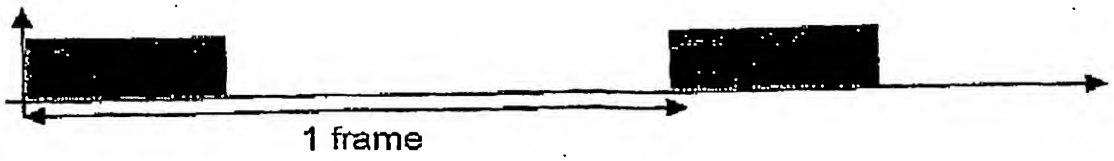


Fig. 5


Fig. 6

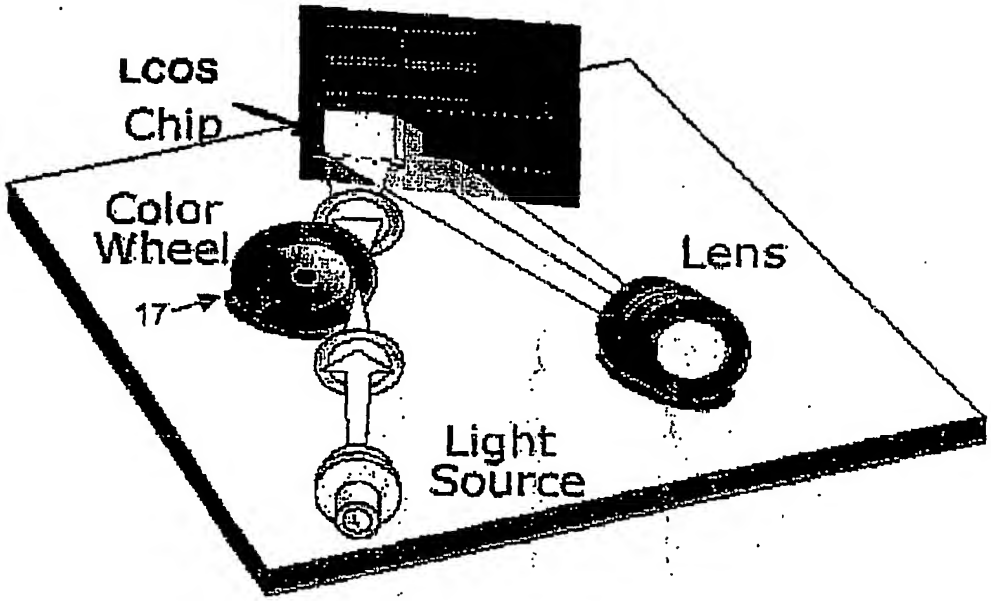


Fig. 7

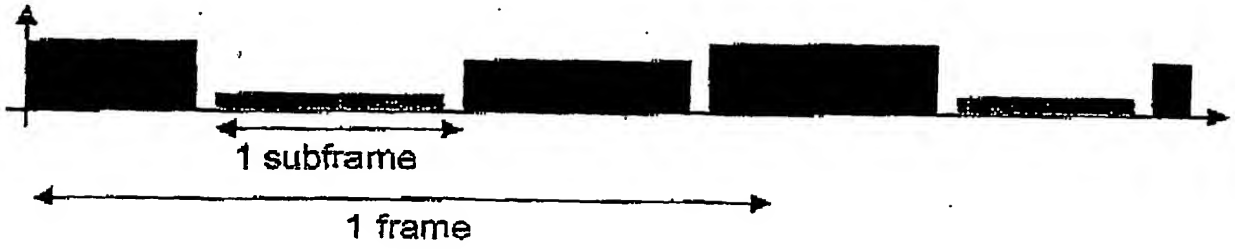


Fig. 8

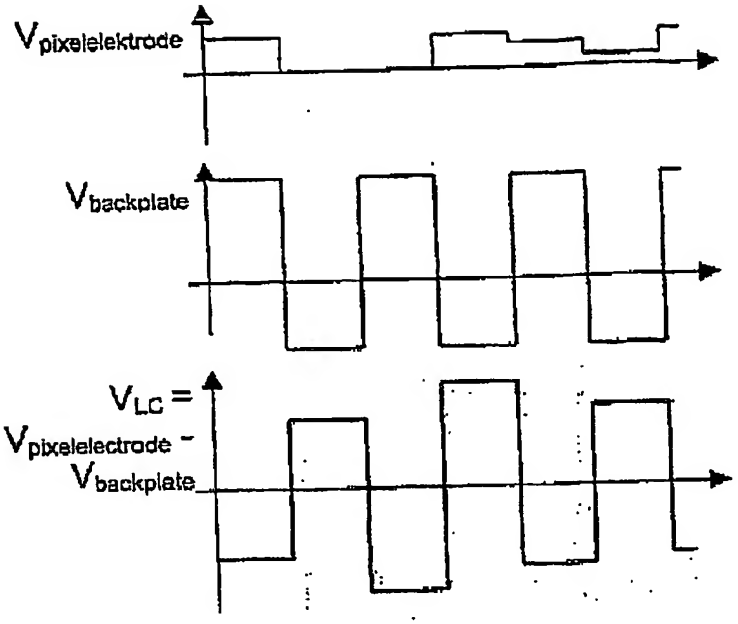
$V_{pixelelektrode}$
$V_{backplate}$
$V_{LC}$ =
$V_{pixelelectrode}$ -
$V_{backplate}$

Fig. 9

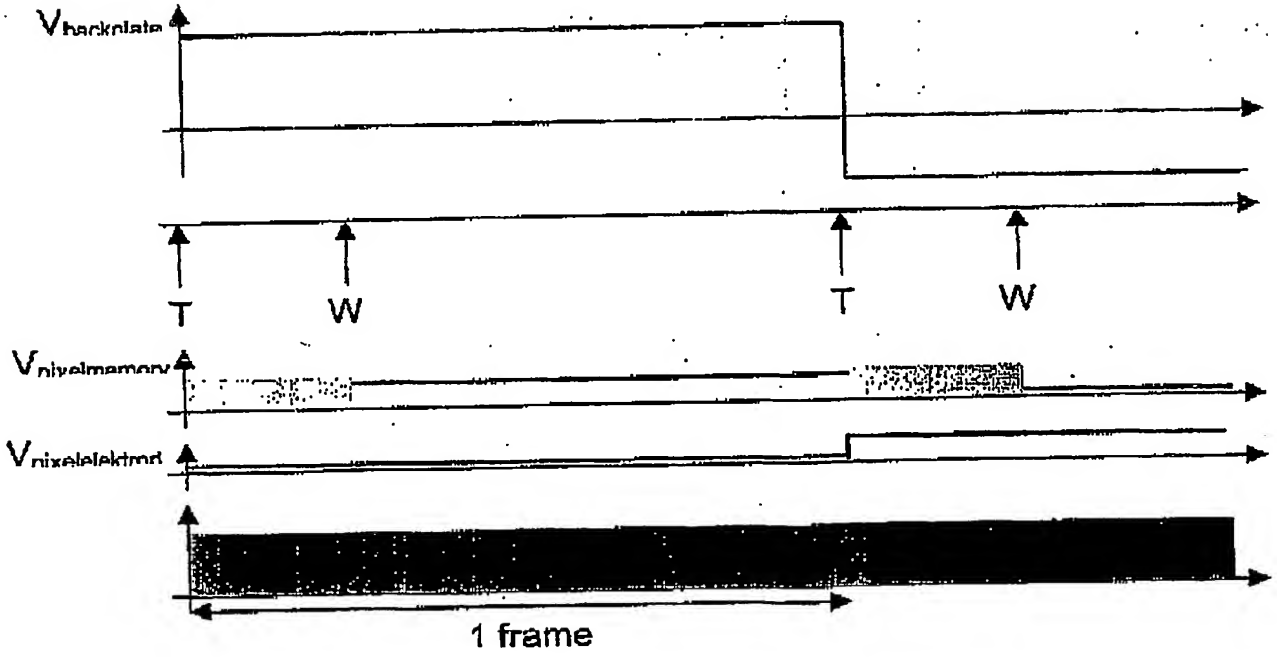
T
W
T
W
1 frame

Fig. 10

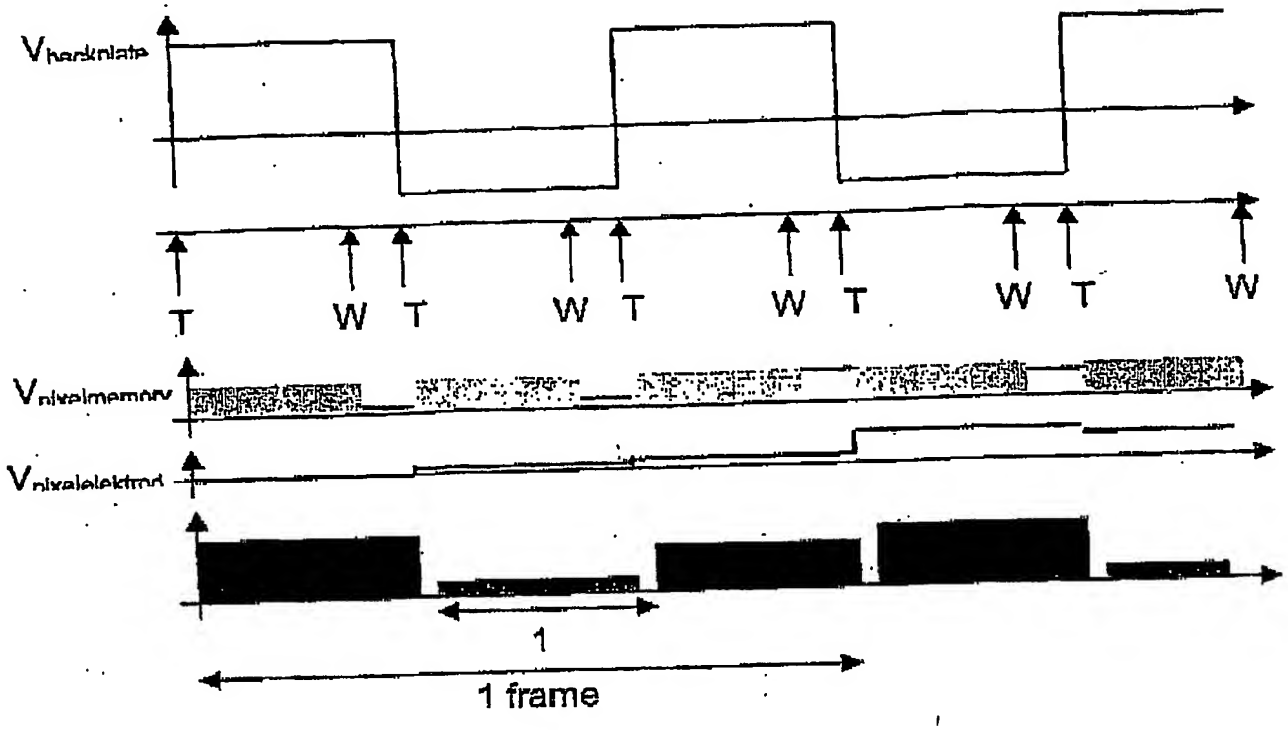
V harklate
T
W T
W T
W T
W T
W
V nivelmemory
V nivelelektrod
1
1 frame

Fig. 11

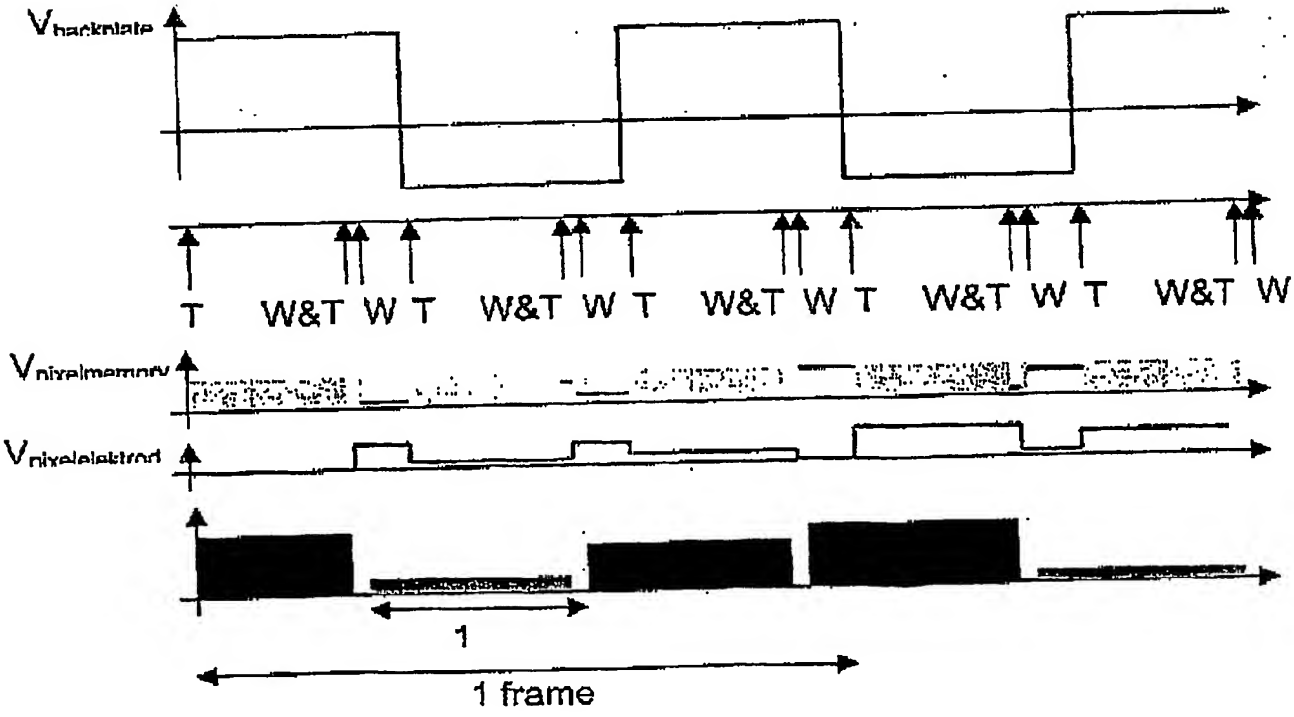
V harklate
T
W&T W T
W&T W T
W&T W T
W&T W T
W&T W
V nivelmemory
V nivelelektrod
1
1 frame

Fig. 12

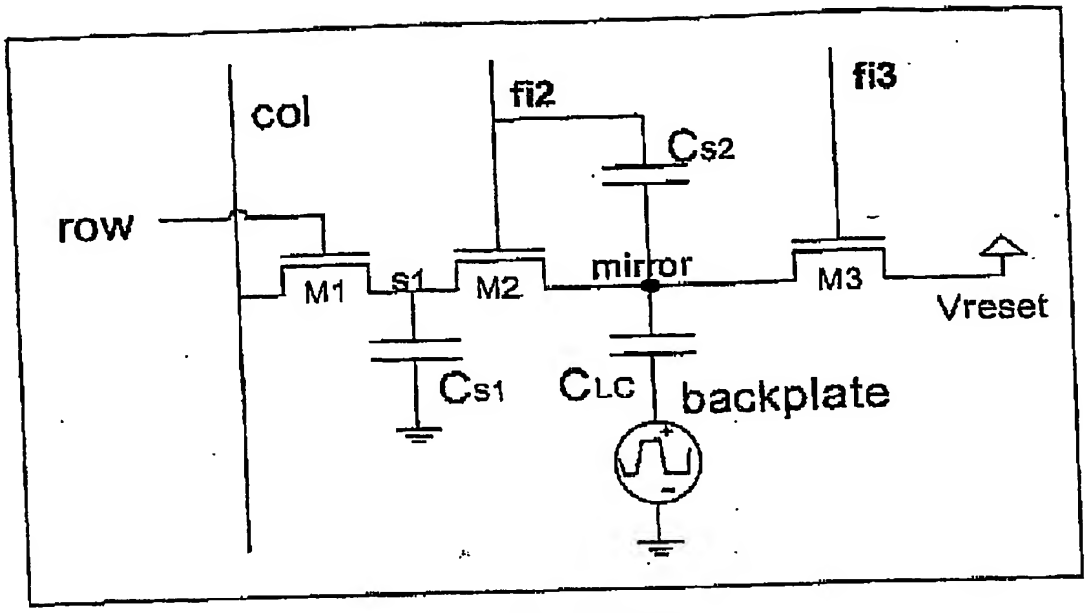
col
fi2
fi3
Cs2
row
M1
s1
M2
mirror
M3
Vreset
Cs1
CLC
backplate

Fig. 13

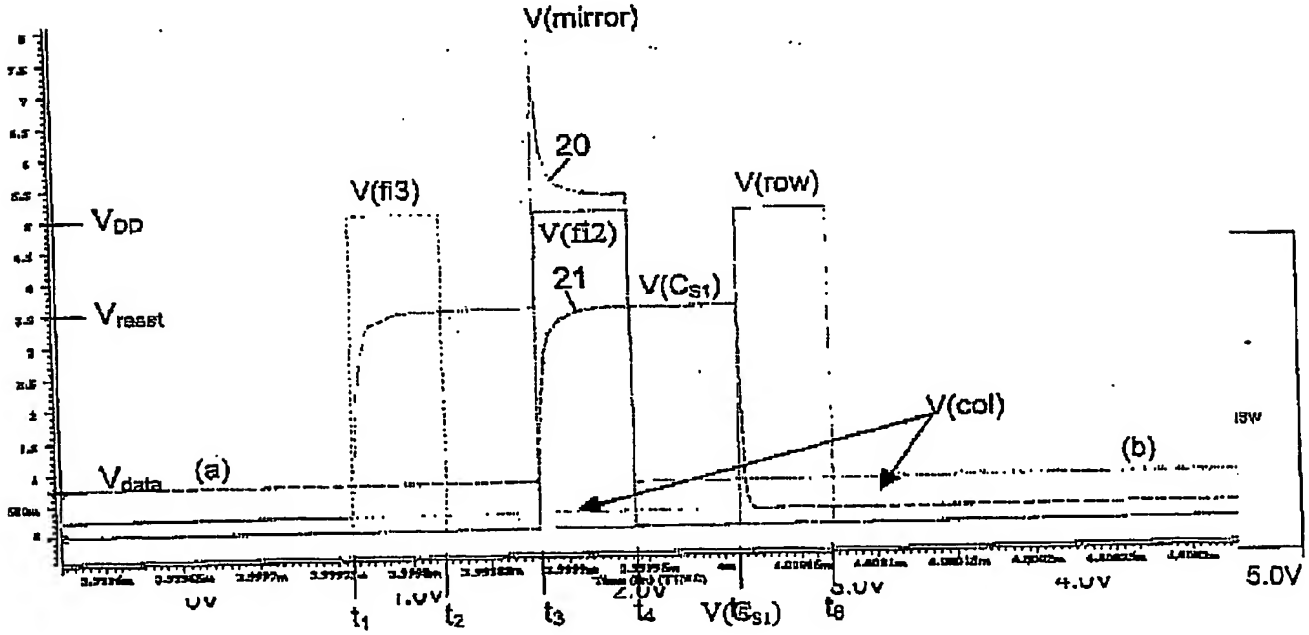
V(mirror)
20
V(fi3)
V(row)
VDD
V(fi2)
21
V(Cs1)
Vreset
V(col)
Vdata
(a)
(b)
0V
1.0V
2.0V
4.0V
5.0V
t1
t2
t3
t4
V(Cs1)
t6

Fig. 15

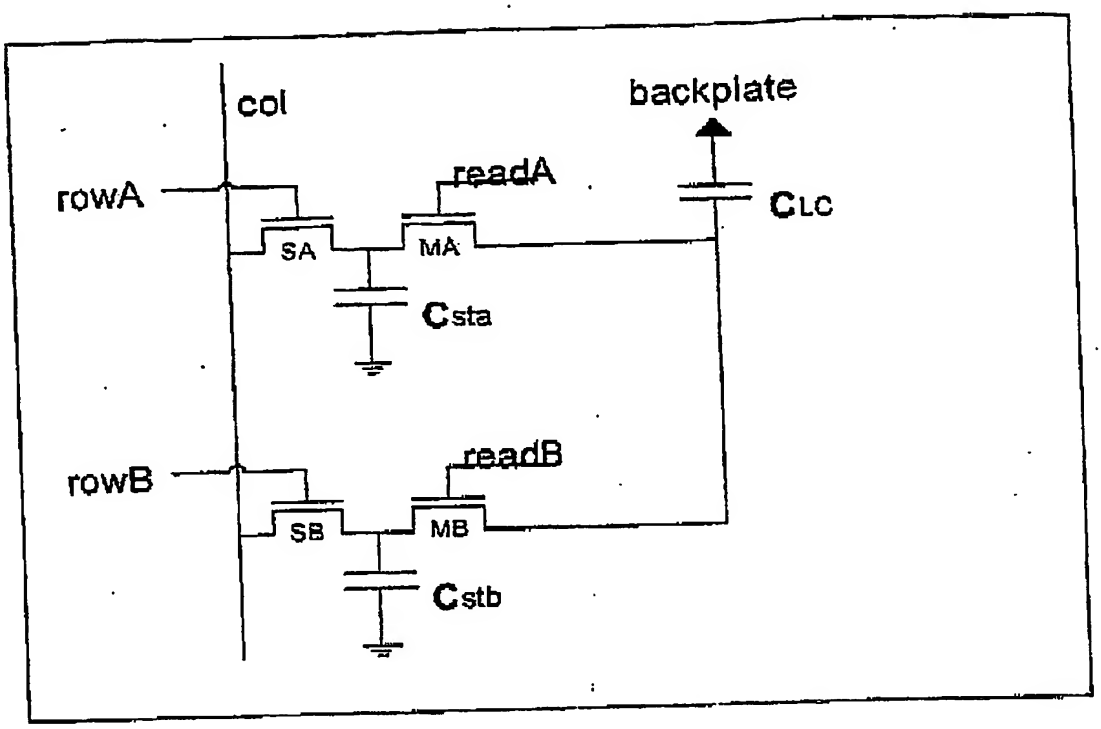
col
backplate
rowA
readA
SA
MA
CLC
Csta
rowB
readB
SB
MB
Cstb

Fig. 16

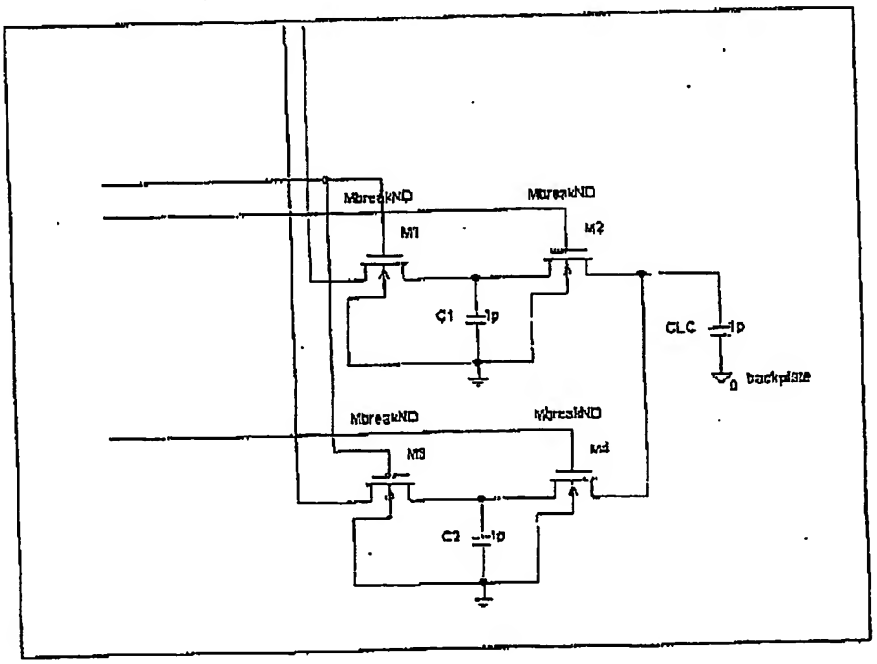
MbreakND
MbreakND
M1
M2
C1 1p
CLC 1p
backplate
MbreakND
MbreakND
M3
M4
C2 1p

Fig. 17

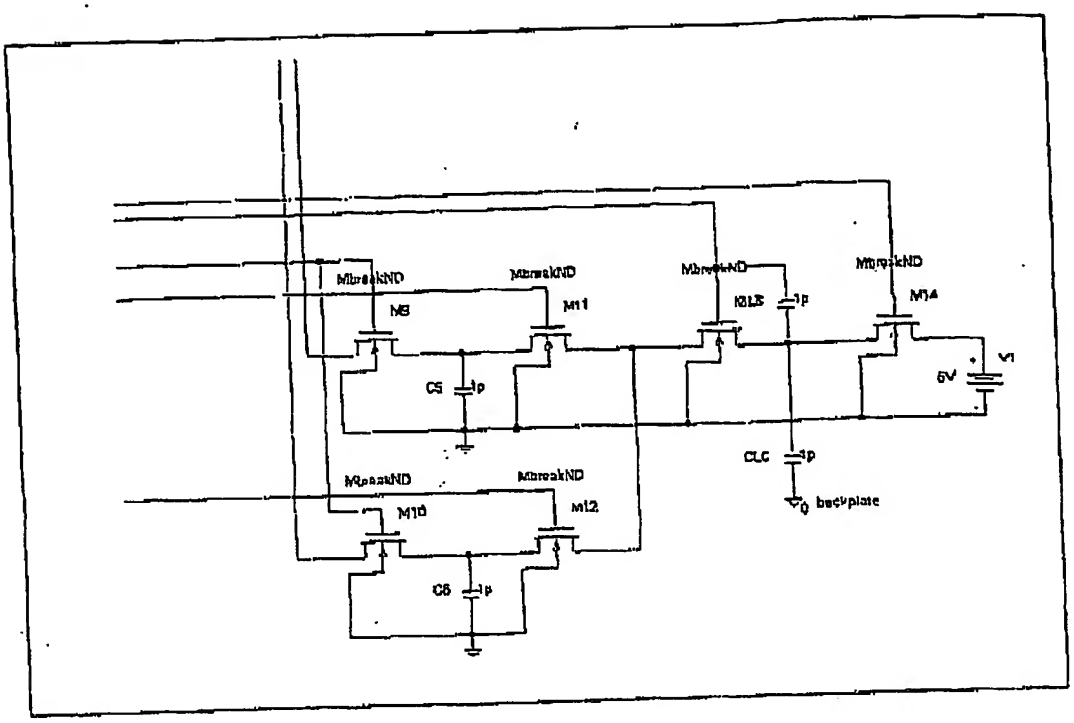
MbreakND
MbreakND
MbreakND
MbreakND
M8
M11
M13
M14
C8 1p
C13 1p
6V
V1
CLC 4p
0 backplate
MbreakND
MbreakND
M10
M12
C6 1p

Fig. 18